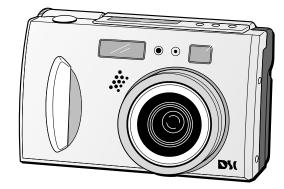
JVC **SERVICE MANUAL**

DIGITAL STILL CAMERA

GC-X1E-S/E-BK/E-BL/E-RD/EK-S/EA



SPECIFICATIONS

Power source Power consumption Dimensions Weight **Operating temperature Relative humidity** Storage temperature LCD screen Storage media CCD Focal distance Lens Video **Recording format** Sensitivity Iris value (F value)

Exposure control Exposure compensation

Shutter speed

White balance

Flash

Focus

Minimum subject distance

Light measurement system

: 4.0 W (when the LCD screen is off) 5.6 W (when the LCD screen is on) : 101 (W) mm x 67 (H) mm x 59 (D) mm

: DC 5 V ----

- (except protruding parts) : Approx. 290 g
- (without a Memory card and battery)
- : 0°C to 40°C
- : 35% to 80%
- : -20°C to 50°C
- : 2.0 inch, polysilicon TFT (200,000 pixels)
- : SmartMedia[™] 3.3V (up to 64MB)
- : 3.34 million pixels (3.24 million valid pixels), 1/1.8" square pixels, primary color filter,
- interlace scan CCD : 7.5 mm to 17.5 mm
- (equivalent to 37mm to 86 mm on a 35 mm still camera) : 2.3X optical zoom lens
- : 160 pixels x 120 pixels, 20 seconds, JVC original format
- : Exif Ver. 2.1 (DCF compliant), TIFF (Uncompressed), DPOF-compatible
- : 80/160/320 (ISO compliant)
- : F2.8/3.8, 5.6, 8, 11
- : Program AE, iris priority AE
- : +/-2EV (0.5EV steps)
- : Approx. 2 cm to 50 cm (in Macro mode) : Multi, spot
- : Built-in.

: Auto/Manual

- Auto/red-eye prevention/forced/disabled Recommended distance for flash : Approx. 2.5 m : Auto (Program AE: 1/8 seconds - 1/750 seconds,
 - Iris priority AE: 1/4 seconds 1/750 seconds) : Auto/Manual (🐑, 🐝, 🛠, MWB, ೨)

Self timer Photo quality Number of storable photos (with an 8MB Memory card, STANDARD/FINE/NO COMP.) Battery Printer connector VIDEO output connector Digital output connector



- : 1 second, 8 seconds
- : 3 modes (STANDARD/FINE/NO COMP.)
- : 2032 x 1536: approx. 10/8/0
- 1024 x 768: approx. 43/32/3 640 x 480: approx. 87/65/8
- : Lithium ion battery
- : Output for optional printer : Two-pole plug, 3.5 mm diameter (PAL)
- · Mini-USB connector

AC Power Adapter/Charger AA-V37

Power requirement		
U.S.A. and Canada	: AC 120 V∼, 60 Hz	
Other countries	: AC 110 V – 240 V∼, 50 Hz/60 Hz	
Power consumption	: 23 W	
Output		
Charge	: DC 3.6 V ==, 0.77 A	
Camera	: DC 5.0 V ==, 1.5 A	
Operating temperature	: 0°C to 40°C [when charging: 10°C to 35°C]	
Dimensions	: 68 (W) mm x 38 (H) mm x 110 (D) mm	
Weight	: Approx. 230 g (without a DC cord)	

E. & O. E. Design and specifications subject to change without notice.

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SOFTWARE SECTION FOR Windows® SOFTWARE SECTION FOR Macintosh® **Operating Environment**

The host computer that runs the Windows® operating environment must satisfy the following conditions.

USB Driver 1. Microsoft[®] Windows[®] 98/Windows[®] 98 Second Edition, pre-installed 2. Available USB port 3. CD-ROM drive

- Video Plaver
- Video Player 1. CPU: Intel® Pentium® 200MHz class or higher 2. Microsoft® Windows® 95/Windows® 98 3. Display capability of 65,536 colors or more 4. CD-ROM drive 5. Minimum RAM requirement: 32MB 6. Minimum hard disk space requirement: 1MB

- * The system requirements information is not a guarantee that provided software applications will work on all personal computers meeting those requirements

- Sorok on all personal computers meeting those requirements.
 * Microsoft[®], Windows[®] are either registered trademarks or trademarks of hilorcosoft corporation in United States and/or other countries of Intel corporation.
 * Intel[®], Pentium[®] are registered trademarks of Intel corporation.
 * Other trademarks are property of their respective owners.
 * If you use Windows[®] 95 or a personal computer which does not have a USB port, use an optional flash path, conversion card adapter, etc. For details on the operating environment of these devices, contact the dealers or manufacturers.

Operating Environment

The host computer that runs the Macintosh® operating environment must satisfy the following conditions.

USB Driver

USB-compatible computer (iMac[™], iBook[™], Power Mac[™] G3/G4, Power Book[™] G3, etc.)
 Mac OS 8.5.1/Mac OS 8.6/Mac OS 9.0

- JVC Video Decoder 1. Power PC 603e/120MHz or faster 2. Mac OS 7.6.1 or later 3. QuickTime 3.0 or later

- QuickTime 3.0 or later
 Minimum RAM requirement: 32MB
 Minimum hard disk space requirement: 1MB

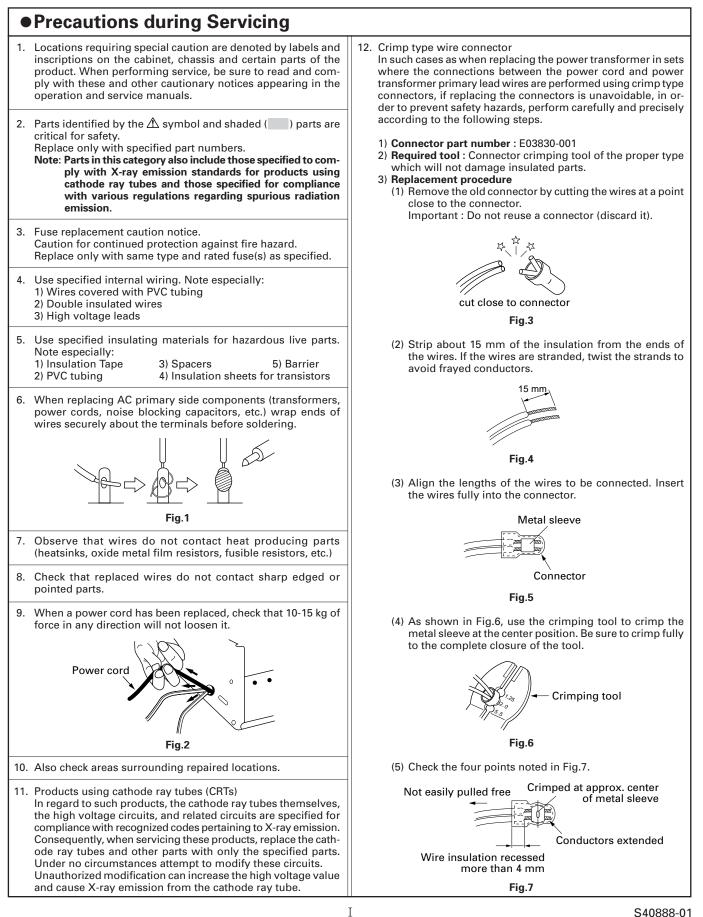
- Macintosh[®] is a registered trademark of Apple Computer.
 Other trademarks are property of their owners.
 If you use Macintosh[®] which does not have a port, use an optional flash path, conversion adapter, etc. For details on the operating en ment of these devices, contact the dealers or manufacturers. manufacturers.

The following table lists the differing points between Models GC-X1E-S, GC-X1E-BK, GC-X1E-BL, GC-X1E-RD, GC-X1EK-S/GC-X1EA in this series.

	E-S	E-BK	E-BL	E-RD	EK-S	EA
AC POWER ADAPTER	AA-V37E	+	+	+	AA-V37EK	AA-V37EA

Important Safety Precautions

Prior to shipment from the factory, JVC products are strictly inspected to conform with the recognized product safety and electrical codes of the countries in which they are to be sold. However, in order to maintain such compliance, it is equally important to implement the following precautions when a set is being serviced.



externally exposed and output terminal Dielectric strength t Confirm specified di accessible parts of th	parts of the set (RF tern	Examine the area surrounding the repaired location for damage or deterioration. Observe that screws, parts and wires have been returned to original positions, Afterwards, perform the following tests and confirm the specified values in order to verify compli- ance with safety standards.					
Confirm specified dia accessible parts of the	Confirm the specified insulation resistance or greater between power cord plug prongs and externally exposed parts of the set (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.). See table 1 below.						
Dielectric strength test Confirm specified dielectric strength or greater between power cord plug prongs and exposed accessible parts of the set (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.). See table 1 below.							
 Clearance distance When replacing primary circuit components, confirm specified clearance distance (d), (d') be- tween soldered terminals, and between terminals and surrounding metallic parts. See table 1 below. Fig. 8 Fig. 8 Fig. 8 Fig. 8 Clearance distance (d) Chassis Fig. 8 Clearance distance (d) Chassis Fig. 8 Chassis Fig. 8 Clearance Comparison Comparison							
and externally expo input and output ter Measuring Method Insert load Z betwee	r lower leakage current sed accessible parts (R minals, microphone jac : (Power ON) en earth ground/power c	between earth ground/po F terminals, antenna termi ks, earphone jacks, etc.). cord plug prongs and extern across both terminals of lo	nals, video and audio	Externally			
Confirm specified or lower grounding impedance between earth pin in AC inlet and externally exposed accessible parts (Video in, Video out, Audio in, Audio out or Fixing screw etc.).Measuring Method: Connect milli ohm meter between earth pin in AC inlet and exposed accessible parts. See figure 10 and grounding specifications.Grounding SpecificationsAC inletOExposed accessible partGrounding SpecificationsRegionGrounding Impedance (Z)USA & CanadaZ ≤ 0.1 ohmEurope & Australia							
Milli ohm meter Fig. 10							
	Fig. 10						
	-	Insulation Resistance (R	Dielectric Stren	nth Clearance Dictance (d) (d')			
AC Line Voltage	Region	Insulation Resistance (R	Dielectric Strens	-			
AC Line Voltage 100 V 100 to 240 V	Region Japan	R≧1 MΩ/500 V DC	AC 1 kV 1 minute AC 1.5 kV 1 miut	e d, d' ≧ 3 mm d, d' ≧ 4 mm			
AC Line Voltage	Region		AC 1 kV 1 minute AC 1.5 kV 1 minute AC 1 kV 1 minute	ed, d' \geq 3 mmed, d' \geq 4 mmed, d' \geq 3.2 mm			
AC Line Voltage 100 V 100 to 240 V	Region Japan	R≧1 MΩ/500 V DC	AC 1 kV 1 minute AC 1.5 kV 1 miut	e d, d' \geq 3 mm e d, d' \geq 4 mm e d, d' \geq 3.2 mm e d \geq 4 mm s II) d' \geq 8 mm (Power cord) d' \geq 8 mm (Power cord)			
AC Line Voltage 100 V 100 to 240 V 110 to 130 V 110 to 130 V	Region Japan USA & Canada Europe & Australia	$R \ge 1 \text{ M}\Omega/500 \text{ V DC}$ $1 \text{ M}\Omega \le R \le 12 \text{ M}\Omega/500 \text{ V }$	AC 1 kV 1 minute AC 1.5 kV 1 minute AC 1 kV 1 minute AC 3 kV 1 minute (Clas AC 1.5 kV 1 minute (Clas	e d, d' \geq 3 mm e d, d' \geq 4 mm e d, d' \geq 3.2 mm e d \geq 4 mm s II) d' \geq 8 mm (Power cord) d' \geq 8 mm (Power cord)			
AC Line Voltage 100 V 100 to 240 V 110 to 130 V 110 to 130 V	Region Japan USA & Canada Europe & Australia	$R \ge 1 \text{ M}\Omega/500 \text{ V DC}$ $1 \text{ M}\Omega \le R \le 12 \text{ M}\Omega/500 \text{ V D}$ $R \ge 10 \text{ M}\Omega/500 \text{ V DC}$	AC 1 kV 1 minute AC 1.5 kV 1 minute AC 1 kV 1 minute AC 3 kV 1 minute (Clas AC 1.5 kV 1 minute (Clas	ed, d' \geq 3 mmied, d' \geq 4 mmed, d' \geq 3.2 mmed \geq 4 mms II)d' \geq 8 mm (Power cord)ted' \geq 6 mm (Primary wire)			
AC Line Voltage 100 V 100 to 240 V 110 to 130 V 110 to 130 V 200 to 240 V	Region Japan USA & Canada Europe & Australia	$R \ge 1 \text{ M}\Omega/500 \text{ V DC}$ $1 \text{ M}\Omega \le R \le 12 \text{ M}\Omega/500 \text{ V DC}$ $R \ge 10 \text{ M}\Omega/500 \text{ V DC}$ Table 1 Specifications for the second	AC 1 kV 1 minute AC 1.5 kV 1 minute AC 1.5 kV 1 minute AC 3 kV 1 minute (Clas AC 1.5 kV 1 minu (Clas each region	ed, d' \geq 3 mmed, d' \geq 4 mmed, d' \geq 3.2 mmed \geq 4 mms II)d' \geq 8 mm (Power cord)s I)d' \geq 6 mm (Primary wire)t (i)a, b, c			
AC Line Voltage 100 V 100 to 240 V 110 to 130 V 110 to 130 V 200 to 240 V	Region Japan USA & Canada Europe & Australia Region	R ≥ 1 MΩ/500 V DC 1 MΩ ≤ R ≤ 12 MΩ/500 V R ≥ 10 MΩ/500 V DC Table 1 Specifications for Load Z \circ —////—•	AC 1 kV 1 minute AC 1.5 kV 1 minute AC 1 kV 1 minute AC 3 kV 1 minute (Clas AC 1.5 kV 1 minu (Clas each region Leakage Current	ed, d' \geq 3 mmed, d' \geq 4 mmed, d' \geq 3.2 mmed \geq 4 mmfII)d' \geq 8 mm (Power cord)titd' \geq 6 mm (Primary wire)t (i)a, b, cExposed accessible parts			
AC Line Voltage 100 V 100 to 240 V 110 to 130 V 200 to 240 V AC Line Voltage 100 V	Region Japan USA & Canada Europe & Australia Region Japan	$R \ge 1 \text{ M}\Omega/500 \text{ V DC}$ $1 \text{ M}\Omega \le R \le 12 \text{ M}\Omega/500 \text{ V DC}$ $R \ge 10 \text{ M}\Omega/500 \text{ V DC}$ Table 1 Specifications for the second	AC 1 kV 1 minute AC 1.5 kV 1 minute AC 1 kV 1 minute AC 3 kV 1 minute AC 3 kV 1 minute AC 1.5 kV 1 minute AC 1.5 kV 1 minute (Class (Class (Class (Class (Class (Class	ed, d' \geq 3 mmed, d' \geq 4 mmed, d' \geq 3.2 mmed \geq 4 mms II)d' \geq 8 mm (Power cord)d' \geq 6 mm (Primary wire)t (i)a, b, cExposed accessible partsesakAntenna earth terminals			

SECTION 1 DISASSEMBLY

1.1 BEFORE ASSEMBLY AND DISASSEMBLY

1.1.1 Precautions

- 1. Be sure to remove the power supply unit prior to mounting and soldering of parts.
- 2. When connecting and disconnecting the connectors, be careful not to damage the wire.
- 3. When replacing chip parts (especially IC parts), desolder completely first (to prevent peeling of the pattern).
- Tighten screws properly during the procedures. Unless specified otherwise, tighten screws at a torque of 0.1N•m (1.0 kgf•cm).

CAUTION!! RISK OF ELECTRIC SHOCK

When disassembling the unit, electric hazards may occur in some cases if the capacitor for strobe emission (STROBE board C6512) has been charged. Therefore be also very careful when performing repairs and inspections.

It is recommended that operations be carried out after waiting for more than ten minutes with the power supply removed or after discharging the capacitor forcibly.

Discharge the capacitor according to <NOTE 2> on Page 1-3.

C6512 is located behind the STROBE board.

PRECAUTIONS ON HANDLING THE LITHIUM SECONDARY BATTERY

This unit is equipped with a coin type lithium secondary battery.

Improper handling of this battery may cause heat to be generated, damage, fires, or leakage. Always follow the precautions below.

- ① Do not short-circuit, disassemble, distort, nor heat the battery.
- ② Load the battery with its + and poles connected correctly.
- ③ Do not solder the battery itself.
- ④ When replacing parts, also refer to the numbers listed in the Parts List of the manual.
- ⑤ Do not store the battery in direct sunlight and hot and humid places.
- 6 When replacing the battery, handle it with care and do not attempt to hold it with tweezers as it may short-circuit.
- When disposing the battery, wind tape around the terminal to insulate the battery, and dispose the battery according to the method prescribed.

1.1.2 Assembly and disassembly

STEP	PART NAME	FIG. NO.	POINT		NOTE
1	FRONT CASE REAR CASE	Fig		Remove screws 2(115), 3(156), 4(114), 1(116)	
2	OPERATION UNIT	1-2-1	Remove the Connector ⓒ MAIN CN4001 ↔ OPERATION UNIT Remove the TOP COVER	Remove screws 3 (116) 2 (115)	NOTE 1
↑ (1)	(2)	↑ (3)	↑ (4)		↑ (5)

- Indicate the disassembly steps. When assembling, perform in the reverse order of these steps. This number corresponds to the number in the disassembly diagram.
- (2) : Indicates the name of disassembly/assembly parts.
- (3) : Indicates the number in the disassembly diagram.
- (4) : Indicates parts and points such as screws, washers, springs which must be removed during disassembly/ assembly.

Lock (L), soldering (SD), shield, connector, etc.

Note: The encircled numbers indicate the order for disassembling the cabinet parts.

The screw numbers indicate the disassembling order. \leftrightarrow :Wire

⇔:Flat wire

← :Board to Bord Connector

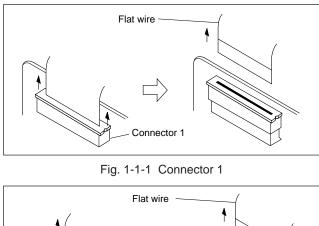
[Example]

- (115) = Remove the parts No 115 screw.
- (SD1) = Desoldering at the point SD1.
- (a) = Disconnect the connector/ML (a) .
- (5) : Precautions on disassembly/assembly.

1.1.3 Disconnection of Connectors (Wires)

Connector

Pull both ends of the connector in the arrow direction, remove the lock and disconnect the flat wire.



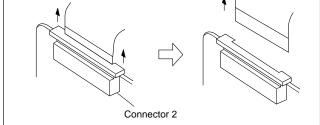


Fig. 1-1-2 Connector 2

Extend the locks in the direction of the arrow for unlocking and then pull out the wire. After removing the wire, immediately restore the locks to their original positions because the locks are apt to come off the connector.

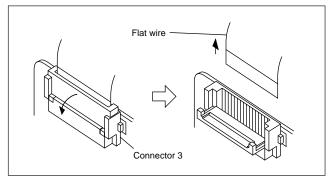
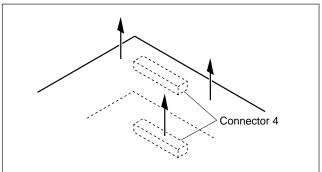


Fig. 1-1-3 Connector 3

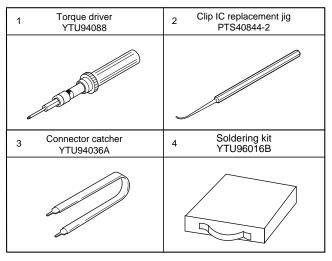
B-B connector

Pull the board by both the sides in the direction of the arrow for disconnecting the B-B connector.



1.2 TOOLS AND EQUIPMENTS REQUIRED FOR ADJUSTMENTS

1.2.1 Tools required for adjustments



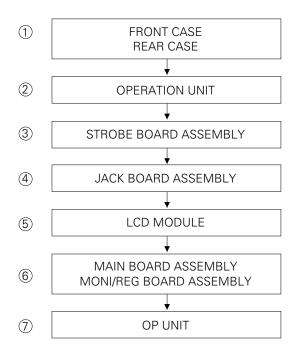
1.3 DISASSEMBLY/ASSEMBLY OF CABINET PARTS

1.3.1 Disassembly flow chart

The following flow chart shows the steps for disassembling the cabinet parts. To assemble, perform the steps of the flow chart in the reverse order.

Note: The encircled numbers indicate the order for disassembling the cabinet parts.

The screw numbers indicate the disassembling order.





1.3.2 Disassembly method (I)

STEP	PART NAME	FIG. NO.	POINT		NOTE
1	FRONT CASE REAR CASE	Fig		Remove screws 2 (115), 3 (156), 4 (157), 1 (154)	
2	OPERATION UNIT	1-3-1	Remove the Connector ⑦ MAIN CN4001 ↔ OPERATION UNIT Remove the TOP COVER	Remove screws 3 (116) 2 (115)	Note 1
3	STROBE BOARD ASSEMBLY	Fig 1-3-1	Remove the Connector (n) MAIN CN6601 ↔ STROBE CN6501	Remove screw 1 (114)	Note 1 Note 2
	JACK BOARD ASSEMBLY		Remove the Connector (\widehat{p}) MAIN CN5501 \iff JACK CN101 (\widehat{m}) LCD MODULE (BL) \iff JACK CN701	Remove screws 2 (114) @ (SD3), (f) (SD4), (f) (SD5)	
4	LCD MODULE	Fig	Remove the Connector (k) MAIN CN3002 ↔ LCD MODULE (LCD) Remove from the Frame Assy Remove from the LCD Holder	Remove screws 2 (114)	Note 1 Note 3 Note 4
5	MAIN BOARD ASSEMBLY MONI/REG BOARD ASSEMBLY	1-3-2	Remove the Connector (h) MAIN CN501 ↔ OP UNIT ⓒ MAIN CN3001 ↔ MON/REG CN9001 ⓓ MON/REG TL9001 ↔ Frame Assy Remove the PWB HOLDER	(d)(SD1) Remove screws 2 (114)	Note 1 Note 1
6	OP UNIT	Fig 1-3-3	Remove from the Frame Assy	Remove screws 3 (117)	

CONNEC- TOR/HL	NO.OF PINS	CON	INECTION
0	80	MAIN Board CN3001	\leftrightarrow MONI/REG Board CN9001
d	1	MONI/REG Board TL9001	\leftrightarrow main frame (red)
e	1	JACK Board TP3	\leftrightarrow main frame (Brown)
f	1	JACK Board TP2	\leftrightarrow MONI/REG Board J9001 (BLACK)
(g)	1	JACK Board TP1	\leftrightarrow MONI/REG Board J9002 (RED)
h	22	MAIN Board CN501	\Leftrightarrow OP UNIT
(j)	2	MAIN Board CN502	\leftrightarrow op unit
k	24	MAIN Board CN3002	\Leftrightarrow LCD MODULE (LCD)
m	2	JACK Board CN701	\Leftrightarrow LCD MODULE (BL)
n	14	MAIN Board CN6601	↔ STROBE Board CN6501
Ø	38	MAIN Board CN5501	\Leftrightarrow JACK Board CN101
(P)	28	MAIN Board CN2001	\leftrightarrow CCD Board CN1001
(1)	12	MAIN Board CN4001	\Leftrightarrow OPERATION UNIT
S	1	STROBE UNIT WIRE (ORANGE	$\dot{z} \rightarrow { m STROBE}$ Board J6501 (Through hole)
t	1	STROBE UNIT WIRE (BROWN)) \leftrightarrow STROBE Board J6502 (Through hole)
U	1	STROBE UNIT WIRE (RED)	\longleftrightarrow STROBE Board J6503 (Through hole)
V	1	STROBE UNIT WIRE (BLACK) \leftrightarrow STROBE Board J6504 (Through hole)
Ŵ	1	STROBE UNIT WIRE (Red, Thin wire	e) \leftrightarrow STROBE Board J6505 (Through hole)
X	1	STROBE UNIT WIRE (BLACK, Thin wire	e) \longleftrightarrow STROBE Board J6506 (Through hole)

Note 1

Destination of connectors.

Note: Three kinds of double-arrows in connection tables respectively show kinds of connector/wires.

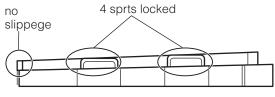
- ← : Board to Board connector
- \Leftrightarrow : Flat wire
- \leftrightarrow : Wire

Note 2

Be careful from electric shock hazard because the capacitor (C6512) for the strobe is exposed. Be sure to positively discharge the capacitor if it is energized by short-circuiting a resistor (10 - 22 k) connected at both capacitor terminals. Please be very careful when doing this job.

Note 3

Make sure that there is no slippage between the LCD panel and the backlight, the four spots are locked with hooks securely, and the sheet is placed in the correct direction.



Note 4

Both the stripe pattern and the non-slippage (notch) on the sheet surface are to be in the direction as illustrated.

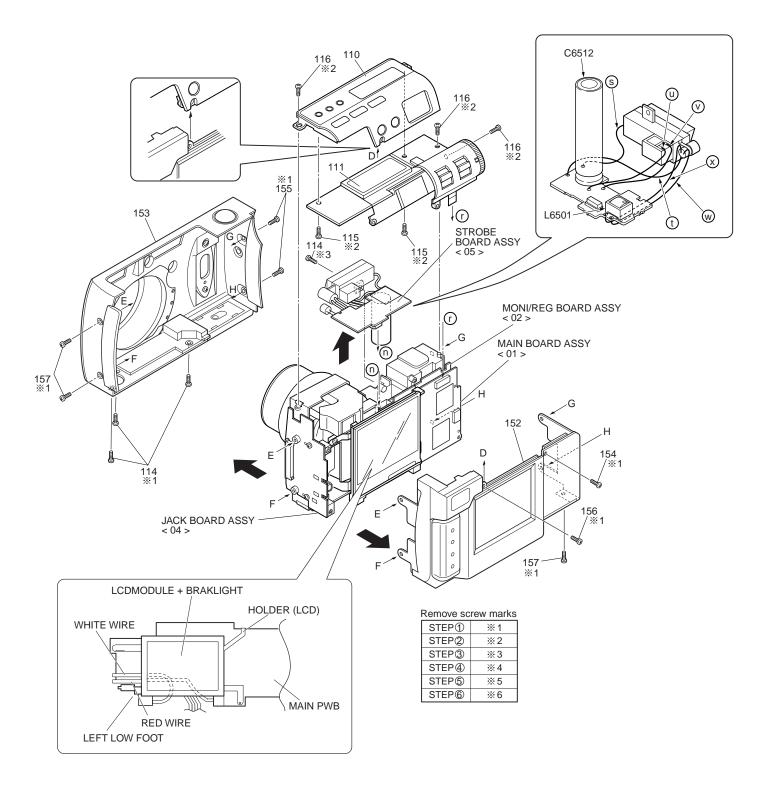


Fig.1-3-1

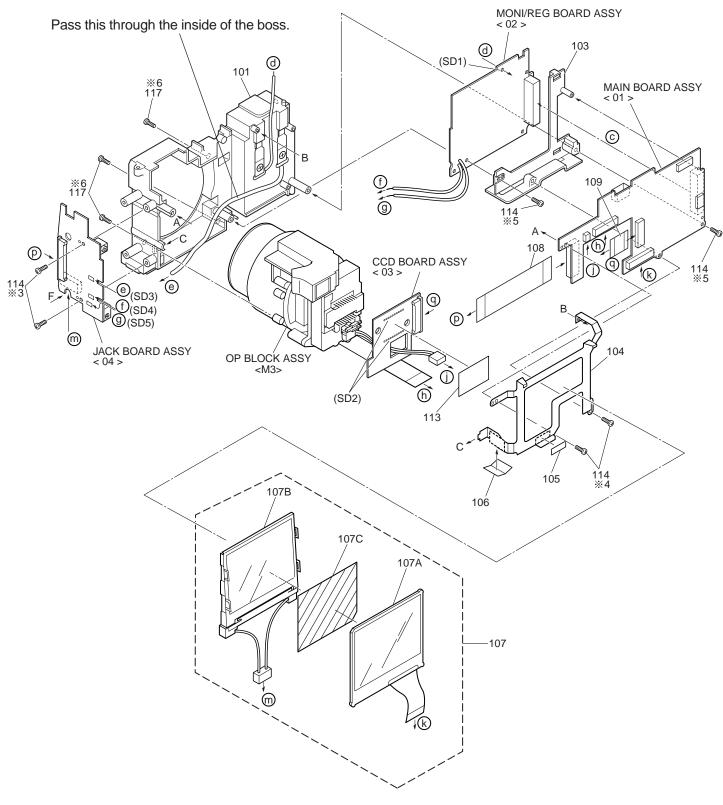


Fig.1-3-2

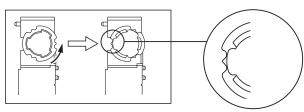
1.3.3 Disassembly method (II) <OP Unit>

STEP	PART NAME	POINT	NOTE
1	OP Block ASSEMBLY	Remove screws 3 (208)	
2	COVER	Remove screws 3 (206),2 (207),	
	CCD BASE ASSEMBLY	1 (236)	
	SPACER	Remove screws 3(206),2(207).	
	SET PLATE	Remove the CCD Board Assy	
		20(SD1)	
3	TILT FRAME	Remove the SET RING	Note 1
	RATCH GEAR	2 (231)	Note 2
	MAIN PIN		Note 3
(4)	RATCH MAGNET	Remove Screws	Note 4
	NUT ASSEMBLY	3 (237),1 (236)	
	RATCH PIECE		

Note 1

×1 208

Turn and fix the set ring and make sure that the convex marks are identical.



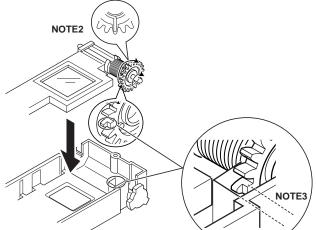
203

Note 2

Make sure that the torsion spring is in the groove of the latch gear.

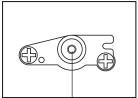
Note 3

Turn the latch gear clockwise (\frown) and position it so that the toothless portion comes to the level that is as high as the main frame.

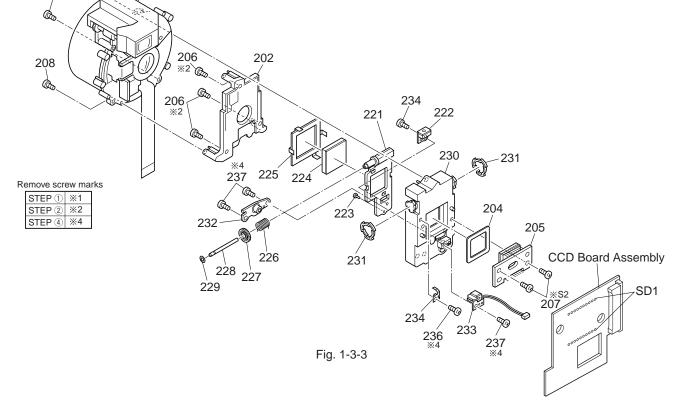


Note 4

Never move the setscrew in the center of the nut assembly!



SET SCREW



1.3.4 OP BLOCK Lens Composition

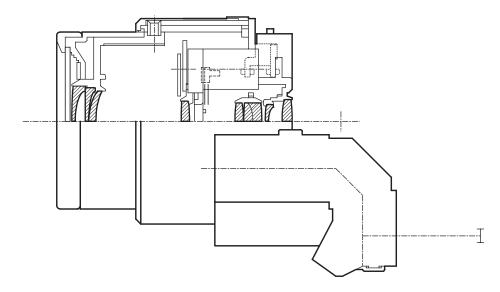


Fig. 1-3-4 Composition of GC-X1E Lens (8-group 9-element lens composition)

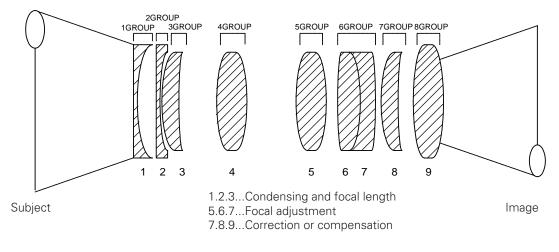
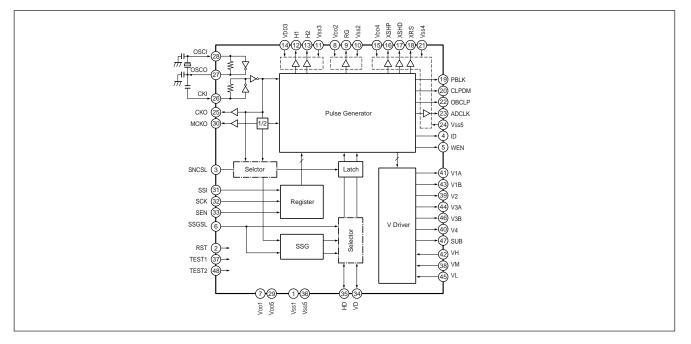


Fig. 1-3-5 8-group-9-piece lens composition

1.4 IC BLOCK DIAGRAM

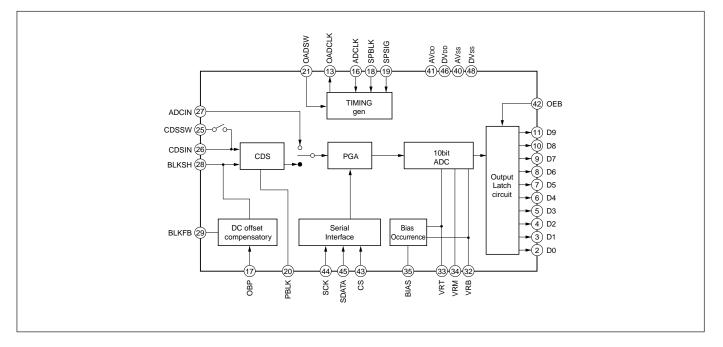
1.4.1 IC 1002 (CXD2497R)



Pin Descriptions

Pin No.	Pin Name	I/0	Description	24	Vss5	-	GND		
1	Vss1	-	GND	25	CKO	0	Inverter output terminal		
2	RST	Ι	System reset input terminal H: Reset released L: Reset	26	CKI		Inverter input terminal		
			activated (Should be activated at power ON, normally.) (Schmitt trigger input/without protection diode on power	27	OSCO	0	Inverter output terminal for oscillation (If not used, should be opened or connected to GND through a capacitor.)		
3	SNCSL		supply side) Sync system switching control input terminal	28	OSCI		Inverter input terminal for oscillation (If not used, should be fixed to "Low".)		
			(with pull-down resistor)	29	VDD5	-	3.3V power (for common logic section)		
			H: CKI sync L: MCKO sync	30	МСКО	0	System clock output terminal for signal processing IC		
4	ID	0	Line identification pulse output terminal in the vertical direction	31	SSI	Ι	Serial interface data input terminal for setting each IC mode (Schmitt trigger input/without protection diode on		
5	WEN	0	Memory write timing pulse output terminal		0.01/	<u> </u>	power supply side)		
6	SSGSL	I	Built-in SSG enable input terminal (with pull-down resistor) H: Built-in SSG is effective. L: External sync is effective.	32	SCK		Serial interface clock input terminal for setting each IC mode (Schmitt trigger input/without protection diode on power supply side)		
7	Voo1	-	3.3V power (for common logic section)	33	SEN		Serial interface strobe input terminal for setting each IC		
8	VDD1 VDD2	-	3.3V power (for RG terminal)		02.1		mode (Schmitt trigger input/without protection diode of		
9	RG	0	Reset gate pulse output terminal for CCD				power supply side)		
10	Vss2	-	GND	34	VD	I/0	Vertical sync signal input/output terminal		
11	Vss3	-	GND	35	HD	I/0	Horizontal sync signal input/output terminal		
12	H1	0	Clock output terminal for CCD horizontal register	36	Vss6	-	GND		
13	H2	0	Clock output terminal for CCD horizontal register	37	TEST1		IC test terminal 1 with pull-down resistor (Should be fixed to GND normally.)		
14	Vdd3	-	3.3V to 5.0V power (for H1 and H2 terminals)	38	VM	-	GND (for vertical drivers)		
15	VDD4	-	3.3V power (for CDS system terminals)	39	V2	0	Clock output terminal for CCD vertical register		
16	XSHP	0	CCD pre-charge level sample/hold pulse output terminal	40	V4	0	Clock output terminal for CCD vertical register		
17	XSHD	0	CCD data level sample/hold pulse output terminal	41	V1A	0	Clock output terminal for CCD vertical register		
18	XRS	0	Sample/hold pulse output terminal for phase matching in analog-to-digital conversion	42	VH	-	15.0V power (for vertical drivers)		
19	PBLK	0	Pulse output terminal for pulse cleaning during	43	V1B	0	Clock output terminal for CCD vertical register		
		-	horizontal and vertical blanking period	44	V3A	0	Clock output terminal for CCD vertical register		
20	CLPDM	0	Pulse output terminal for CCD dummy signal clamping	45	VL	-	-7.5V power (for vertical drivers)		
21	Vss4	-	GND	46	V3B	0	Clock output terminal for CCD vertical register		
22	OBCLP	0	Pulse output terminal for CCD optical black signal	47	SUB	0	Pulse output terminal for CCD electronic shutter		
23	ADCLK	0	Clock output terminal for analog-to-digital conversion IC Logical phase is adjustable with the serial interface data	48	TEST2		IC test terminal 2 with pull-down resistor (Should be fixed to GND normally.)		

1.4.2 IC 2001 (CDS/AGL)

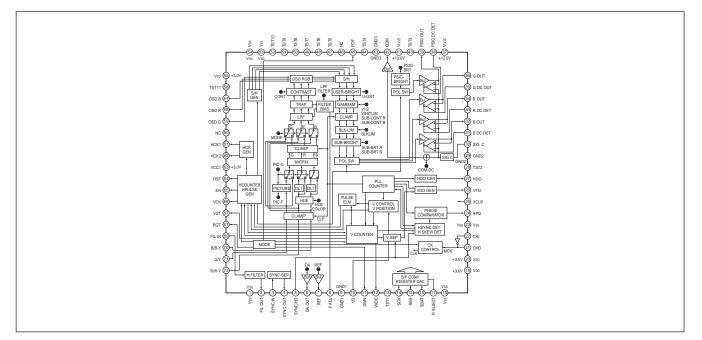


Pin Descriptions

Pin No.	Pin Name	Description	I/0	Analog (A) or Digital (D)
1	NC	No internal connection	-	-
2	D0	Digital output terminal (LSB)	0	D
3-10	D1-D8	Digital output terminals	0	D
11	D9	Digital output terminal (MSB)	0	D
12	NC	No internal connection	-	-
13	OADCLK	Latch clock output terminal for D0 to D9	0	D
14	DVss	Digital GND (0V)	-	D
15	DVdd	Power for digital 3.0V system (Should be connected to AVDD outside the IC.)	-	D
16	ADCLK	Analog-to-digital conversion clock input terminal		D
17	OBP	Optical black pulse input terminal		D
18	SPBLK	Black level sampling clock input terminal		D
19	SPSIG	Signal level sampling clock input terminal		D
20	PBLK	Pre-blanking signal input terminal		D
21	OADSW	OADCLK enable input terminal		D
22	AVss	Analog GND (0V)	-	A
23	AVdd	Power for analog 3.0V system	-	A
24	NC	No internal connection	-	-
25	CDSSW	Signal level sampling output terminal	0	A
26	CDSIN	CDS input terminal		A
27	ADCIN	ADC input terminal		A
28	BLKSH	Black level sample/hold terminal	-	A
29	BLKFB	Black level feedback terminal	-	A
30	AVss	Analog GND (0V)	-	A
31	AVdd	Power for analog 3.0V system (Should be connected to DVDD outside the IC.)	-	A
32	VRT	Reference voltage terminal 3 (Ceramic capacitor of 0.1µF or more should be connected between this terminal and AVss.)	-	A
33	VRB	Reference voltage terminal 2 (Ceramic capacitor of 0.1µF or more should be connected between this terminal and AVss.)	-	A

34	VRM	Reference voltage terminal 1	-	А
		(Ceramic capacitor of 0.1µF or more should		
		be connected between this terminal and AVss.)		
35	BIAS	Internal bias terminal	-	A
		(A 24-Kohm resistor should be connected		
		between this terminal and AVss.)		
36	NC	No internal connection	-	-
37	AVss	Analog GND (0V)	-	А
38	AVdd	Power for analog 3.0V system	-	А
		(Should be connected to DVDD outside the IC.)		
39	NC	No internal connection	-	-
40	AVss	Analog GND (0V)	-	А
41	AVdd	Power for analog 3.0V system	-	А
		(Should be connected to DVDD outside the IC.)		
42	OEB	Digital output enable control input terminal	Ι	D
43	CS	Serial interface control input terminal	Ι	D
44	SCK	Serial clock input terminal	Ι	D
45	SDATA	Serial data input terminal		D
46	DVdd	Power for digital 3.0V system	-	D
		(Should be connected to AVDD outside the IC.)		
47,48	DVss	Digital GND	-	D

1.4.3 IC 7302 (CXA3268AR)



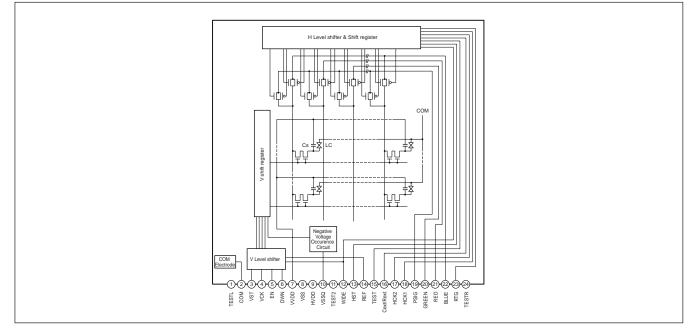
Pin Descriptions

Pin No.	Pin Name	I/0	Description	Input Res.
1	Vss	-	GND terminal for digital 3.0V system	
2	FIL OUT	0	H filter output terminal (for internal sync separator use)	
3	SYNC IN	Ι	Sync input terminal for sync separator circuit (for internal sync separator use)	
4	SYNC OUT	0	Sync output terminal for sync separator circuit (for internal sync separator use)	
5	CSYNC/HD	Ι	CSYNC/horizontal sync signal input terminal	
6	DA OUT	0	DAC output terminal	
7	REF	0	Level shifter circuit reference voltage output terminal for LCD panel	
8	F ADJ	0	f0 adjust resistor connecting terminal for TRAP	
9	GND1	-	GND terminal for analog 3.0V system	
10	VD		Vertical sync signal input terminal	L
11	DWN	0	Up/Down switching signal output terminal	
12	WIDE	0	16:9 wide display switching pulse output terminal	
13	TST1	-	Test terminal (Should be opened.)	
14	SCK		Serial clock input terminal	
15	SEN	Ι	Serial load input terminal	
16	SDAT		Serial data input terminal	
17	R INJECT	0	Resistor connecting terminal for serial block current control	
18	Vss	-	GND terminal for digital 3.0V system	
19	Vdd	-	Power for digital 3.0V system	
20	Vdd	-	Power for digital 3.0V system	
21	СКО	0	Oscillation cell output terminal	
22	CKI		Oscillation cell input terminal	
23	Vss	-	GND terminal for digital 3.0V system	
24	RPD	0	Phase comparison output terminal	
25	XCLR	Ι	Capacitor connecting terminal for power-on reset (for timing generating system)	Η
26	VDO	0	VDO pulse output terminal	
27	HDO	0	HDO pulse output terminal	
28	TST2	-	Test terminal (Should be connected to GND.)	
29	GND2	-	GND terminal for analog 12.0V system	
30	SIG.C		DC voltage adjust terminal for R, G, B and PSIG outputs	
31	B DC DET	0	Capacitor connecting terminal for B signal's DC voltage feedback circuit	
32	B OUT	0	B signal output terminal	
33	R DC DET	0	Capacitor connecting terminal for R signal's DC voltage feedback circuit	
34	R OUT	0	R signal output terminal	
35	G DC DET	0	Capacitor connecting terminal for G signal's DC voltage feedback circuit	

	0.000	•							
36	G OUT	0	signal output terminal						
37	Vcc2	-	Power for analog 12.0V system						
38	PSIG DC DET	0	Capacitor connecting terminal for G signal's DC voltage feedback circuit						
39	PSIG OUT	0	PSIG output terminal						
40	TST3	-	Test terminal (Should be opened.)						
41	Vcc3	-	Power for analog 12.0V system COM (CS)						
42	COM	0	Common electrode voltage output terminal (CS) for LCD panel						
43	GND3	-	GND terminal for analog 12.0V system COM (CS)						
44	TST4	-	Test terminal (Should be opened.)						
45	POF	0	LCD panel power ON/OFF terminal (Open, if this function is not used.)						
46	NC	-	No internal connection						
47	TST5	-	Test terminal (Should be connected to GND.)						
48	TST6	-	Test terminal (Should be connected to GND.)						
49	TST7	-	Test terminal (Should be opened.)						
50	TST8	-	Test terminal (Should be opened.)						
51	TST9	-	Test terminal (Should be opened.)						
52	TST10	-	Test terminal (Should be opened.)						
53	Vss	-	GND terminal for digital 3.0V system						
54	Vss	-	GND terminal for digital 3.0V system						
55	Vdd	-	Power for digital 3.0V system						
56	TST11	-	Test terminal (Should be connected to GND.)						
57	OSD B	Ι	OSD B input terminal						
58	OSD R	Ι	OSD R input terminal						
59	OSD G	Ι	OSD G input terminal						
60	NC	-	No internal connection						
61	HCK1	0	H clock pulse 1 output terminal						
62	HCK2	0	H clock pulse 2 output terminal						
63	Vcc1	-	Power for analog 3.0V system						
64	HST	0	H start pulse output terminal						
65	EN	0	EN pulse output terminal						
66	VCK	0	V clock pulse output terminal						
67	VST	0	V start pulse output terminal						
68	RGT	0	Right/Left switching signal output terminal						
69	FIL IN		H FILTER input terminal (for internal sync separator use)						
70	B/B-Y		B/B-Y signal input terminal						
71	G/Y	Ι	G/Y signal input terminal						
72	R/R-Y		R/R-Y signal input terminal						

* DWN: <u>DOWN</u> SCAN and UP SCAN H: Pull-up resistor incorporated RGT: <u>RIG</u>HT SCAN and LEFT SCAN L: Pull-down resistor incorporated

1.4.4 LCD (ACX301AK)



Pin Descriptions

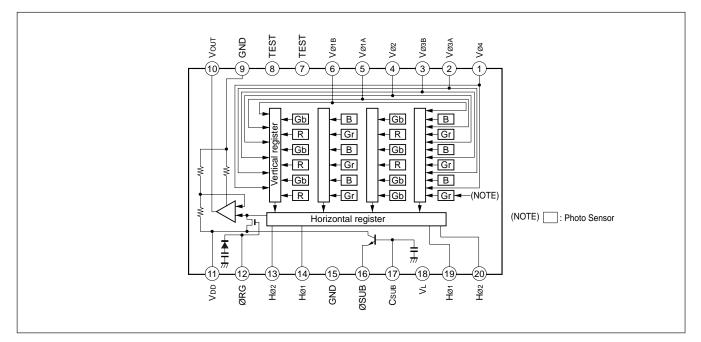
Pin No.	Pin Name	Description
1	TESTL	Panel testing terminal (Should be opened.)
2	COM	Common electrode voltage input terminal for panel
3	VST	Start pulse input terminal for V shift register drive
4	VCK	Clock input terminal for V shift register drive
5	EN	Enable signal input terminal for gate select pulse
6	DWN	Drive direction signal input terminal for V shift register
7	VVdd	Power for V driver
8	Vss	GND for H and V drivers
9	HVdd	Power for H driver
10	VSSG	Negative voltage setting terminal for V driver
11	TEST2	Connected to GND through a 1-Mohm resistor in the panel
12	WIDE	Pulse input terminal for 16:9 mode
13	HST	Start pulse input terminal for H shift register drive
14	REF	Level shifter circuit reference voltage input terminal
15	TEST	Panel testing terminal (Should be opened.)
16	Cext/Rext	Power input terminal for setting H shift register drive time constant
17	HCK2	Clock input terminal for H shift register drive
18	HCK1	Clock input terminal for H shift register drive
19	PSIG	Uniformity improving signal input terminal
20	GREEN	Video signal (G) input terminal for the panel
21	RED	Video signal (R) input terminal for the panel
22	BLUE	Video signal (B) input terminal for the panel
23	RGT	Drive direction signal input terminal for H shift register
24	TESTR	Panel testing terminal (Should be opened.)

Features

- Device Structure
 - Active matrix panel with internal driver using low-temperature polysilicon transistors
- Pixels
 Total dots: 896 (H) x 230 (V) =206,080
 Display dots: 880 (H) x 228 (V) =200,640 (2.0 in.)
- Total dots: 200,000 dots 5.1cm diagonal (2.0 in.)
- Horizontal resolution: 440 TV scanning lines
- Light permeability: 5.6% (standard)
- Smooth screen image with RGB delta array
- NTSC/PAL compatible
- High image quality internal circuitry
- 16:9 screen display function
- Low-reflection screen display processing assures easy viewing even outdoors
- Anti-grime display

F	2	C	3	E	3	F	2	C	3	E	3	
	E	3	F	2	0	5	E	3	F	२	(3
F	ζ	C	3	E	3	F	ζ	C	3	E	3	
	E	3	F	२	0	5	E	3	F	२	(L)
F	ς	C	3	E	3	F	ς	C	3	E	3	

Delta array



Pin Descriptions

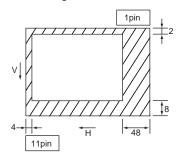
Pin No.	Pin Name	Description
1	Vø4	Vertical register transfer clock
2	Vøза	Vertical register transfer clock
3	Vøзв	Vertical register transfer clock
4	Vø2	Vertical register transfer clock
5	Vø1A	Vertical register transfer clock
6	Vøзв	Vertical register transfer clock
7	TEST	Test terminal*1
8	TEST	Test terminal*1
9	GND	GND
10	Vout	Signal output
11	Vdd	Circuit power
12	øRG	Reset gate clock
13	Hø2	Horizontal register transfer clock
14	Hø1	Horizontal register transfer clock
15	GND	GND
16	øSUB	PCB clock
17	Csub	PCB bias ^{*2}
18	VL	Protection transistor bias
19	Hø1	Horizontal register transfer clock
20	Vø2	Horizontal register transfer clock

*1: Terminal should be opened.

*2: A $0.1\mu F$ capacitor should be connected between the pin and GND, since the DC bias is generated inside the CCD.

Features

- Field period readout system
- Interline CCD image sensor
- Total number of pixels: 2140 (H) x 1560 (V) approx. 3340k pixels
- Number of effective pixels: 2088 (H) x 1550 (V) approx. 3240k pixels
- Effective number of pixels: 2080 (H) x 1542 (V) approx. 3210k pixels (1.18in)
- Chip size: 8.10mm (H) x 6.64mm (V)
- Unit cell size: 3.45m m (H) x 3.45m m (V)
- Optical black: Horizontal (H) direction : front 4 pixels, rear 48 pixels Vertical (V) direction : front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28 Vertical 1 (even fields only)
- Square pixels
- Horizontal drive frequency: 18kHz
- RGB basic color mosaic on-chip color filter
- High sensitivity
- Cyclic, variable speed shutter
- Excellent anti-blooming characteristics



Optical black wiring diagram (Top View)

SECTION 2 ELECTRICAL ADJUSTMENT

2.1 ELECTRICAL ADJUSTMENT

2.1.1 Precautions

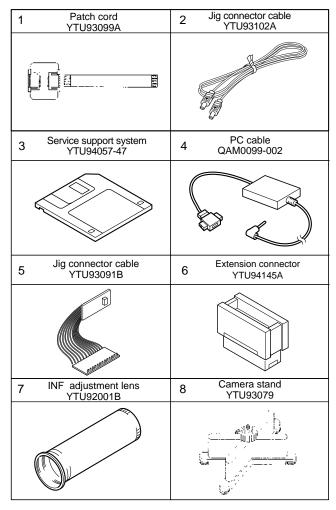
Both the camera section and deck section of this model are designed and manufactured to be adjustment-free. However, if both or either of the following parts is replaced, it needs special adjustment with a personal computer at a JVC service equipment after the part replacement

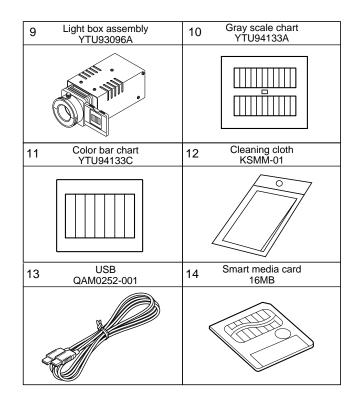
- OP block assembly
- EEPROM (on the MAIN board)

When there is some trouble in the electric circuit, it is required to detect the faulty part with specified test instruments first and then to proceed to repair, replacement and adjustment.

- When cheking a signal at a chip test point, be sure to use an IC clip or the like not to apply any stress to the test point. When replacing a chip part (IC in particular), completely remove solder chips from it and its periphery before proceeding to part replacement (in order to avoid exfoliation of the pattern).
- 2. Carefully disconnect/connect connectors because they are apt to get damaged.

2.1.2 Test instruments required for electrical adjustment





2.1.3 Required test equipment

- 1. Color TV monitor.
- 2. AC power adapter (AA-V37 or equivalent)
- 3. Oscilloscope (dual-trace type, for more than 20 MHz).
- 4. Digital voltmeter
- 5. Frequency counter (with threshold level adjuster)
- 6. Personal computer

2.1.4 Setup (LCD ADJUSTMENT)

Setup for electrical adjustment with personal computer

Note 1: As a general rule for adjustment with a personal computer, connect a personal computer to its PRINTER terminal.

Note 2: Use DC cord to supply the power.

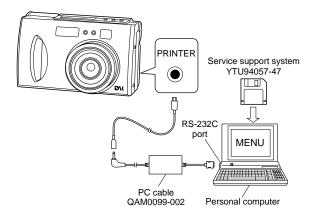


Fig. 2-1-1 Setup for electrical adjustment with personal computer (I)

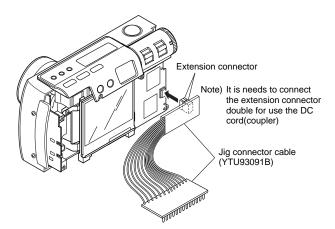


Fig. 2-1-2 Setup for electrical adjustment with personal computer (II)

Pin No.	FUNCTION
1	135TMS
2	135TDI
3	nTRST
4	AL_3.3V
5	32DBI
6	GND
7	M_COM
8	M_SIG_C
9	M_RED
10	M_SIG_GND
11	JTAGMODE
12	135TDO
13	135TCK
14	AL_3.3V
15	32RST
16	M_BLUE
17	RPD
18	M_PSIG
19	M_GREEN
20	NC

Table 2-1-1 Jig Connector Function

2.1.5 Setup (CCD ADJUSTMENT)

Setup for electrical adjustment with personal computer

Note 1: As a general rule for adjustment with a personal computer, connect a personal computer to its DIGITAL terminal.

Note 2: Use DC cord to supply the power.

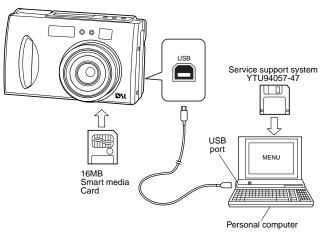


Fig. 2-1-3 Setup for electrical adjustment with personal computer (I)

2.2 Setup with patch cords and jig connector cables

Note:

Fig. 2-2-1 shows an example of expansion setup that facilitates inspection of major boards because main components are connected by means of patch cords and jir cables. For proceeding to electrical adjustment in such the setup, disassemble the set at certain level required for the current adjustment objectives referring to the section 1 "DISASSEMBLY" and properly set up the expanded set and test instruments.

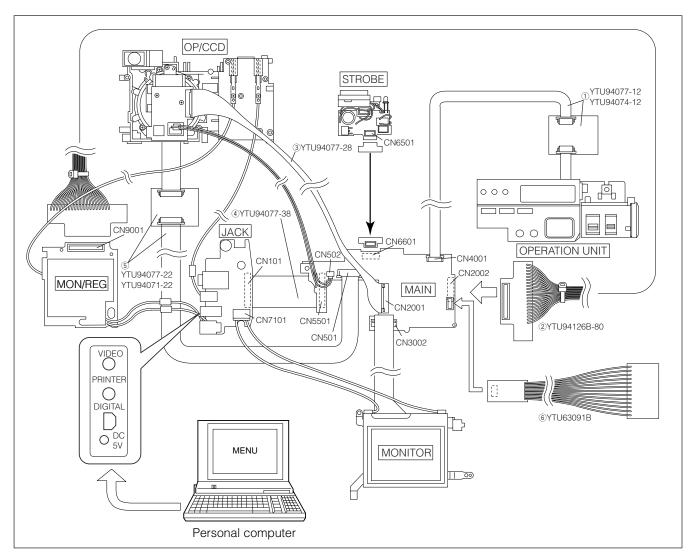


Fig. 2-2-1

		Connection		Pin No.	Parts Number		
1	MAIN CN4001	\leftrightarrow	OPRATION UNIT		12	YTU94077-12	FPC wire
						YTU94074-12	FPC CN.ASSY
2	MAIN	\leftrightarrow	MON/REG	CN9001	80	YTU94126B-80	B TO B CN.ASSY
3	MAIN CN2001	\longleftrightarrow	CCD	CN1001	28	YTU94077-28	FPC wire
(4)	MAIN CN5501	\leftrightarrow	JACK	CN101	38	YTU94077-38	FPC wire
5	MAIN CN501	\longleftrightarrow	OPUNIT		22	YTU94077-22	FPC wire
						YTU94074-22	FPC CN.ASSY
6	MAIN CN2202	\longleftrightarrow			20	YTU93091B	JIG CN.cable



S40894

